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A Star-Connected Rectifier Employed by the Three-Phase Interleaved LLC Resonant Converter Used by the High-Efficiency Isolated AC–DC Converter

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Abstract—
The power conversion efficiency of an isolated ac–dcconverter is a dominant factor in the overall efficiency of dc distri-bution systems. To improve the power conversion efficiency of the dc distribution system, a three-phase interleaved full-bridge LLC resonant converter employing a Y-connected rectifier is proposed as the isolated ac–dc high-frequency-link power-conversion system. The proposed Y-connected rectifier has the capability of boosting the output voltage without increasing the transformer's turn ratio. Especially, the frequency of the rectifier's output ripple is six times higher than the switching frequency, thereby reducing the output capacitor and the secondary transformer's RMS current. However, the tolerance of the converter's resonant components in each pri-mary stage causes the unbalance problem of output ripple current. It cannot be solved using conventional control techniques since the structure of the three-phase interleaving has the limitations of in-dividual control capability for each converter. To solve the current unbalance problem, a current balancing method is proposed for the output rectifying current. The performance of the proposed con-verter and the current balancing method has been verified through experiments using a 10 kW (300 V/33.3 A) prototype converter.

Index Terms—Current balancing method, high-frequencypower interface, LLC resonant converter, three-phase interleaved, Y-connected rectifier.

I. INTRODUCTION

N MODERN times, a tremendous growth in telecommunica-Ition and data storage systems has resulted in the installationof millions of internet data center (IDC) around the globe. As the volume of data centers and servers has grown, the overall amount of electricity consumption also increased. Power distri-bution systems in a typical data center consist of several power conversion stages. Especially, electrical power is delivered using an ac grid system that goes through multiple power conversions between ac and dc. Each power conversion increases powerlosses, which wastes energy, produces heat, and requires a data center's heavy cooling system.

The conventional several power delivery architectures which use ac or dc voltage have been presented in [1]. A conventional ac power distribution system of the IDC consists of four power conversion stages with a traditional online uninterrupted power supply (UPS), which employs an ac–dc–ac double conversion.

Compared with the ac distribution system, the dc distribution system does not need several power conversion stages such as the online UPS and the individual power factor correction (PFC) circuit in front of each power supply unit (PSU) [2]–[6]. Therefore, the dc distribution system for the data centers can reduce the power conversion loss caused by redundant power stages [7], [8]. Furthermore, in order to obtain high-power conversion efficiency of the dc distribution system, the high-efficient isolated ac–dc converter used in the dc distribution system should decrease its power loss [9]–[11]. The galvanic isolation in the power conversion stage is not more popular than the isolation of the server level; however, it is one of interesting research topics of isolation applications for IDC since the safety from an electric shock can be required for the operators who are achieving the maintenance operations of the servers.

An isolated conventional ac–dc converter consists of two power conversion stages. The primary power conversion stage is generally designed to a nonisolated ac–dc rectifier for PFC operation. A boost PFC operating under the continuous con-duction mode (CCM) is commonly used in ac–dc high-power applications. When the boost PFC operates under the CCM, the reverse recovery time of the boost rectifier diode causes the reverse

recovery current which increases the power loss. In order to reduce this power loss of the CCM PFC rectifier, the reverse recovery current of the rectifying diode should be reduced. To solve this reverse recovery problem, various soft-switching techniques using additional passive or active snubber circuits have been proposed [12]–[16]. However, those methods require relatively large number of passive or active components which increase the production cost of the system. Moreover, the complex structure of the rectification circuit with many switch-ing components decreases the reliability of the overall power conversion system. An alternative method to minimize those drawbacks is the use of SiC diodes instead of conventional diodes in the rectification circuit [17], [18]. The SiC diode has very small reverse recovery current. Therefore, it can re-duce the power loss caused by the reverse recovery current. Conventional full-bridge diodes used on the front side of the PFC circuit also increase conduction losses. Various bridgeless PFC topologies have been proposed for eliminating the full-bridge diode rectifier [19]–[24]. Those topologies can get rid of the line-current path and can decrease the conduction loss caused by the full-bridge diode.

The power density of an isolated dc–dc converter for the dc power distribution systems is one of the significant performance indicator, since the size of the desired system is limited. There-fore, multiple medium power converters connected in parallel, which share load current to increase the amount of power con-version is proper rather than a single large converter employing parallel switching devices with a big isolation transformer. A full-bridge phase shift converter is a frequently selected topol-ogy for high power dc–dc applications [25]–[27]. In order to increase the converter's rated power using parallel operations, the parallel connection methods for the output stages using mul-tiple phase-shift converters have been proposed [28], [29]. How-ever, these topologies cannot accomplish zero-voltage switching (ZVS) under light load conditions and additional filter inductors for the output rectifier are required. The LLC resonant converter is another popular topology because of its outstanding perfor-mance such as high-power conversion efficiency, high power density, and its ZVS capability over the entire load range. Mul-tiphaseLLC resonant converters have also been developed to reduce the output ripple current [30]–[34]. Since an interleaved operation for the LLC resonant converter has been adopted, the output ripple current and the size of the filter capacitors could be reduced. However, those conventional studies have concentrated on the low output voltage and high-output current applications using a center-tapped transformer. The number of

turns in the secondary winding used for the center-tap structure is twice the turn number required for the full-bridge structure [35]. Since the output voltage needed for the dc distribution system is relatively high (e.g., 300 to 400 V), the center-tap structure is not suitable for high-output voltage applications.

A three-phase interleaved LLC resonant converter employing a Y-connected rectifier is proposed in this paper. The proposed converter consists of three full-bridge LLC resonant convert-ers whose output stage is composed of Y-connected three-phase full-bridge diode rectifiers for each secondary transformer wind-ing. It has ZVS capability over the entire load range similar to the conventional LLC resonant converter. In addition, the proposed Y-connected rectifier can boost the output voltage without in-creasing the transformer's turn ratio. Especially, the frequency of the rectifier's output ripple is six times higher than the switching frequency, thereby reducing the output capacitor and the RMS current of the transformer's secondary winding. Therefore, the proposed converter is suitable for high-power and high-output voltage applications. However, the imbalance of resonant net-works in the LLC resonant converters can cause the unbalance phenomena of output rectifying current. It cannot be solved us-ing conventional control techniques since the structure of the three-phase interleaving has the limitation of individual control capability for each converter.

In this paper, the high efficiency isolated ac–dc converter will be discussed to improve the performance of the dc distribution system. The proposed isolated ac–dc converter is
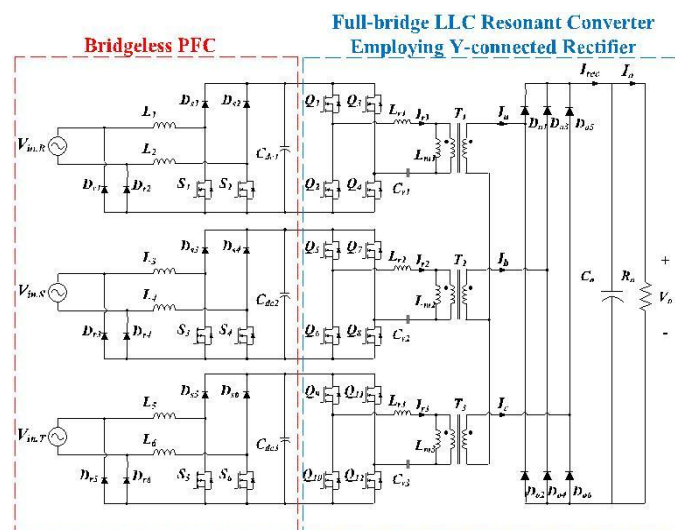

Fig. 1.Circuit diagram of the proposed isolated ac–dc high-frequency-link power-conversion system.

composed of the high-efficiency bridgeless PFC rectifier with the SiC diodes, and the three-phase interleaved full-bridge LLC resonant converter with the Y-connected rectifier. In addition, an output current balancing method for the three-phase interleaved LLC resonant converter will be proposed. The performance ofthe proposed ac–dc high-frequency-link power-conversion sys-tem will be experimentally verified using a 10 kW prototype converter.

II. PROPOSED AC–DC HIGH-FREQUENCY-LINK
POWER-CONVERSION SYSTEM

The proposed ac–dc high-frequency-link power-conversion system is composed of three bridgeless PFC rectifiers and a three-phase interleaved LLC resonant converter. Fig. 1 shows the schematic of the proposed isolated ac–dc converter. To im-prove power conversion efficiency, the CCM bridgeless boost PFC rectifier using the SiC diodes has been designed. The in-put power source of the proposed ac–dc converter is three-phase four-wired ac. Therefore, three 3.3 kW (380 V/8.7 A) PFC boost rectifiers have been designed for 220 Vac input voltage. Each of the rectifier is controlled by a commercial analog controller. In addition, the three-phase interleaved full-bridge LLC resonant converter using the Y-connected rectifier is proposed for high-efficiency dc–dc power conversion and galvanic isolation. The proposed converter is controlled by a single digital signal pro-cessor (DSP). The proposed current balancing algorithm is also implemented by the same DSP. The detailed circuit operations of the proposed converter will be discussed in this Section.

A. Bridgeless PFC

As shown in Fig. 1, a bridgeless PFC with a dual boost method is used for the first stage of the proposed system. The topology is the best choice in medium-to-high power applications since it has a simple current-sensing circuit, low conduction loss, and
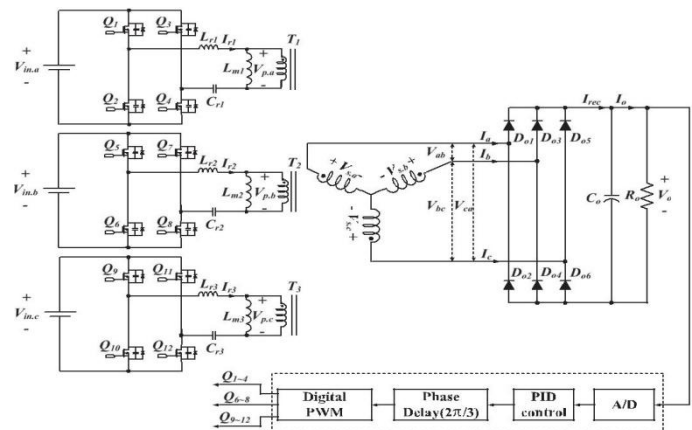

Fig. 2.Schematic of the proposed three-phase interleaved LLC resonant con-verter with DSP control.

small EMI noise [19]. In addition, two power switches can be driven using the same PWM signal. In the input side rectifier diodes, D_r , slow recovery diodes can be used for each half-line cycle. In order to reduce the reverse recovery phenomena, the SiC diodes are used for the boost rectifier diodes, D_s . The detailed operation of this bridgeless PFC is shown in [20]. As a result, three bridgeless PFC rectifier has been designed with the SiC diode and the dual boost method to improve the power-conversion efficiency of the proposed system. For
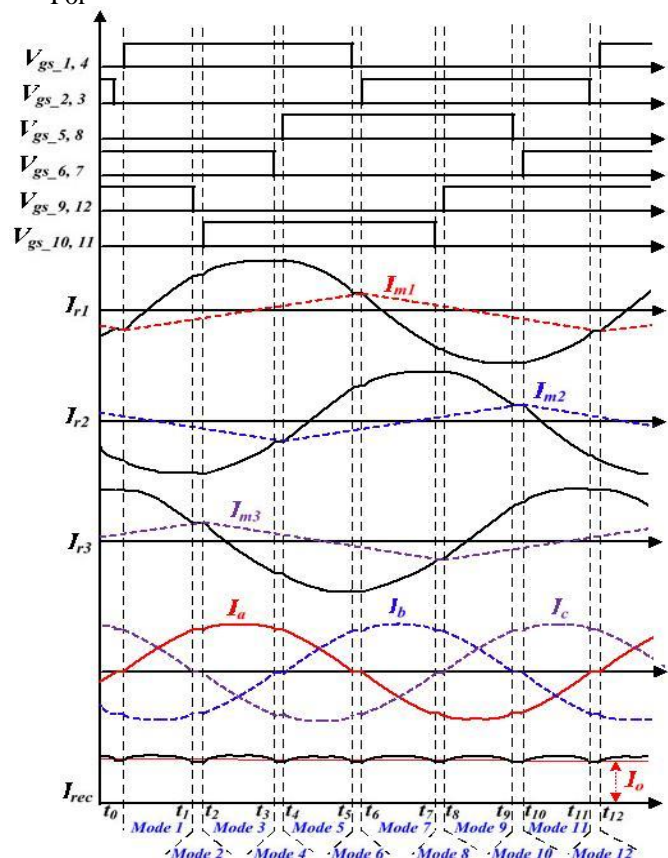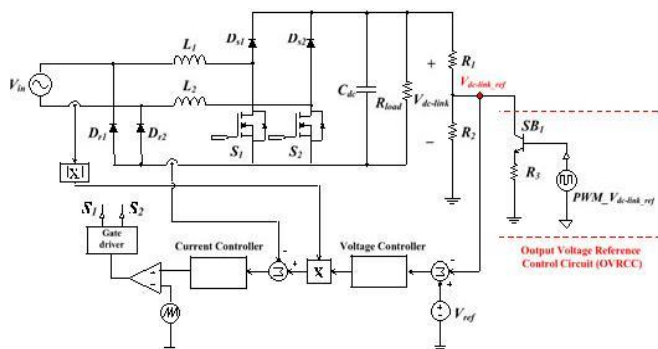
Fig. 8.Schematic of PFC rectifier with the control circuit of output voltage reference.

the three-phase interleaved LLC resonant converter employing the Y-connected rectifier is required to compensate the unbal-anced current. The detail description of the proposed current balancing algorithm using a reference control circuit will be presented in the next Section.

IV. PROPOSED CURRENT BALANCING METHOD

A. Rectifying Current Balancer Based on DC-Link Voltage Compensation

As explained in the aforementioned Section, the unbalance phenomena of the rectifying current in the proposed converter are influenced by the gain difference of each converters'reso-nant network. When the input voltage of the converter is fixed, the unbalance problem cannot be solved using the conventional PFM controller because of the limitations of individual control capability for each converter, which means the same switching frequency for all converters. If another controller is able to con-trol the output voltages of bridgeless PFCs, the difference of the resonant gain can be compensated by adjusting input voltages of each converter. In addition, this method can control each output rectifier current passing through the output filter capacitors in the Y-connected rectifier.

Fig. 8 shows the propose control strategy of the bridgeless PFC using the control circuit of output voltage reference. The control circuit is a hybrid voltage controller based on a con-ventional analog voltage controller of PFCs with digital control signal generated from a DSP. If all of the bridgeless PFC con-verters can be controlled by the DSP controller, the balancing algorithm will be easily implemented because the controller has a advantage of easily adjustable output voltage reference. However, this method requires additional voltage and current sensing circuits, which convert analog signals to isolated digital signals for the DSP using the proposed three-phase interleaved Y-connected LLC resonant converter with Y-connected rectifier. In addition, this method also increases the

computational bur-den of the DSP controller and the production cost of the ac–dc high-frequency-link power-conversion system.

As shown in Fig. 8, the proposed bridgeless PFC circuit is controlled by an analog PFC controller. In order to adjust the output voltage of the bridgeless PFC, an output voltage reference control circuit (OVRCC) is proposed. It is simply composed of a bipolar junction transistor, a resistor, and a PWM signal, PWM Vdc−link ref , generated from the DSP con-troller. When the duty ratio of PWM Vdc−link ref increases, the OVRCC decreases Vdc−link ref , consequently, the analog PFC controller will increase the output voltage of the bridgeless PFC. On the other hand, the voltage controller will decrease the output voltage of the bridgeless PFC when the duty ratio of PWM Vdc−link ref decreases for reducing the reference volt-age. Using OVRCC, the output voltage of PFCs, which is the input voltage of the proposed *LLC* resonant converter, can be controlled by the DSP controller.

In order to prevent unstable and uncontrollable conditions in the output voltage of PFCs, it is limited by a hardware protec-tion circuit as resisters R1 ,R2 , and R3 , which determined the output voltage reference Vdc−link ref . When the duty ratio of PWM Vdc−link ref is zero, the maximum voltage of Vdc−link ref can be derived as following the equation:

$$V_{dc-link\ ref.} = \frac{R_1}{R_2} \times V_{dc-link} \quad . (\quad 7 \quad)$$

From (7), the output voltage of PFCs is limited to the mini-mum voltage. When the duty ratio of PWM Vdc−link ref is max-imum, Vdc−link ref falls to the minimum voltage as shownnext

$$V_{dc-link-ref} = \frac{R_1}{R_2 // R_3} \times V_{dc-link} \quad . (\quad 8 \quad)$$

Therefore, the output voltage of PFCs is limited to the maxi-mum voltage. Actually, the variation of the PFCs' output voltage under overall load variation is enough about ±5% from the ex-perimental results. Therefore, the minimum output voltage of PFCs is limited to 360 V. In addition, the maximum output volt-age of PFCs is limited to 400 V. The proposed LLC resonant converter is designed to be able to accommodate the change of input voltage about ±20 V. In addition, the proposed LLC resonant converter and the proposed bridgeless PFC rectifier are controlled independently. Therefore, the unstable condition caused by the proposed balance methods can be prevented.

For controlling output rectifier current, the peak value of the output rectifier current should be measured. Fig. 9 shows the peak current sensing circuits of the proposed converter using current transformers (CTs). Using CTs in the secondary stage of the Y-connected rectifier, the amplitude of each output rectifier current can be measured. These sensing signals are transferred to the DSP controller to calculate the peak value of each output rectifier current.

B. Algorithm Implementation Using DSP-Based Control System

Figs. 10 and 11 show the proposed current balancing algo-rithm and the control scheme of the algorithm, respectively. The current balancing algorithm is implemented using the DSP con-troller which also controls the output voltage of the proposed dc–dc converter. According to the magnitude of the peak value of the rectifier current, the proposed current balancing circuit changes each output voltage of the PFC circuits. As shown in Fig. 10, if the difference among the sensed rectifying currents of each converter is over a specific threshold, the middle value
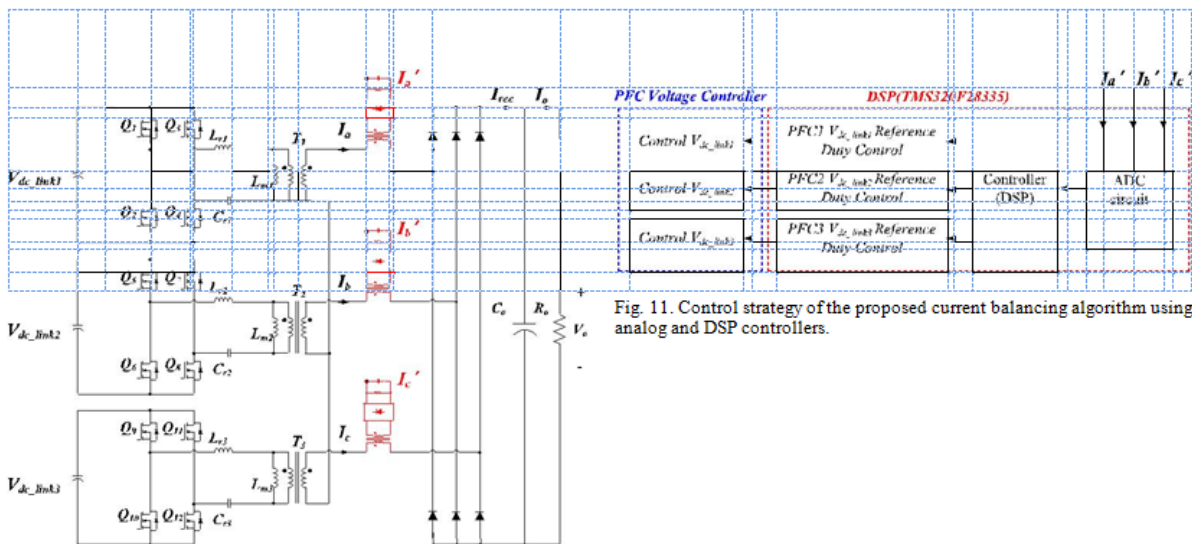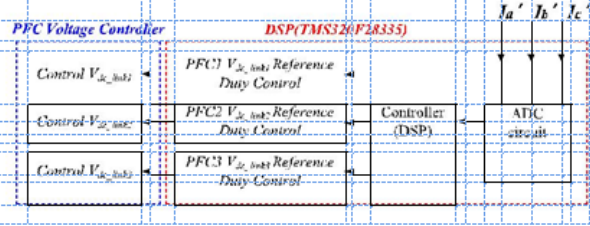

Fig. 11. Control strategy of the proposed current balancing algorithm using analog and DSP controllers.

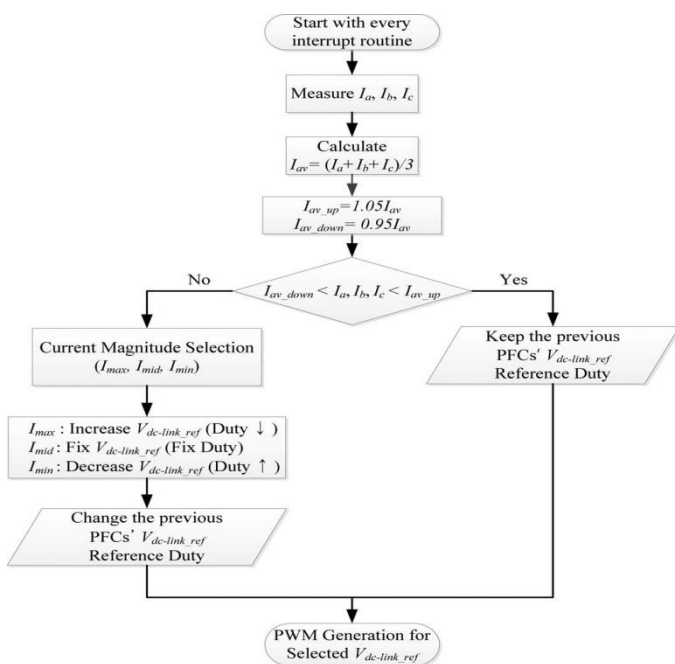Fig. 9.Peak current sensing circuits of the secondary stage of the proposed converter.
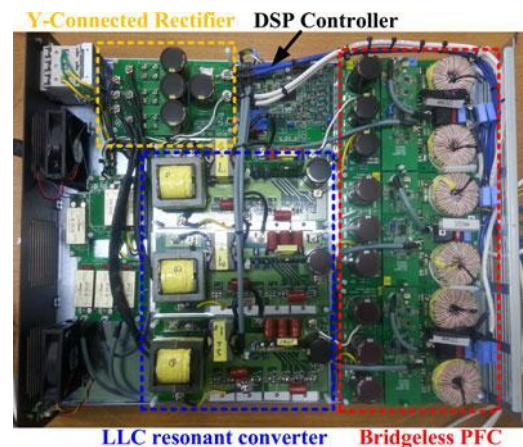

Fig. 10.Proposed current balancing algorithm.

Fig. 12. Prototype of the proposed 10 kW isolated ac–dc high frequency-link power-conversion system.

TABLE I
DESIGN SPECIFICATIONS OF THE PROTOTYPE
BRIDGELESS PFC CONVERTER

Specifications	Values
Input Voltage (V_{in})	AC 220V
Output Voltage (V_{out})	DC 380V
Rated Power (P_{out})	3.3kW × 3
PFC Control IC	L4981
Main Switch (S)	IXKR47N60C5
Rectifier Diode (D_r)	DSEI2X101-06
Boost Diode (D_s)	C3D20060D
Boost Inductance $(L_1 = L_2)$	800 μH

verter is higher than other converters. In the case of the minimum rectifier current, the PFC' output voltage should be increased because the resonant gain of this converter is lower than other converters. Using the proposed balancing algorithm, the difference of the resonant gain among LLC resonant converters can be compensated. As a result, the unbalanced output rectifier current can be regulated.

V. EXPERIMENTAL RESULTS

Fig. 12 shows the prototype of the proposed isolated ac–dc high-frequency-link power-conversion system. Tables I and II show the designed parameters of the prototype PFC and dc–dc converters, respectively. The input power source of the proposed converter is composed of three-phase and four wire AC. The rated output power of the proposed system is 10 kW.
Three 3.3 kW (380 V/8.7 A) bridgeless PFC rectifiers have been designed for 220 Vac input voltage. The boost inductors.

TABLE II
DESIGN SPECIFICATIONS OF THE ROTOTYPE
THREE-PHASE INTERLEAVEDLLC
RESONANT CONVERTER

Specifications	Values
Input Voltage (V_{in})	DC 380V
Output Voltage (V_{out})	DC 300V
Rated Power (P_{out})	10kW
Switching Controller	TMS320F28335
Main Switch (Q)	IXKR47N60C5
Rectifier Diode (D_o)	DSEI2X101-06
Transformer Core	EE6565 (ISU PM7)
Transformer Turns Ratio $(N_1 : N_2)$	27 : 9
Operating Frequency (f_s)	34 ~ 39kHz
Magnetizing Inductance (L_m)	470μH
Resonant Inductance (L_r)	120μH
Resonant Capacitance (C_r)	141nF
Output Capacitance (C_o)	(680μF/450V) × 4

designed as $L_1=L_2=$ 800μ H were implemented using a commercial toroidal core (CH571125, Chang-sung). The switching frequency was 50 kHz and the PFC's power stage op-erated in the CCM using a commercial controller L4981 made by STmicroelectonics. The output voltage of the PFCs is nor-mally regulated to 380 V. When the PFCs are controlled by the proposed unbalance control algorithm using the OVRCC, the output voltages of PFCs can be changed from 360 to 400 V.

A 10-kW (300 V/33.3 A) prototype dc–dc converter was designed to test the performance and validity of the pro-posed current balancing algorithm. The transformer turn ra-tio of *LLC* resonant converter, *n*, is 27:9. According to a fixed primary turn number, the secondary turn number of the conventional full-bridge *LLC* resonant converter with the full-bridge rectifier requires double as the turn number of the proposed converter. Under balanced condition, the reso-nant components of three *LLC* resonant converters designed to

$L_{m1}= L_{m2}= L_{m3}=$ 470μH$,L_{r1}=L_{r2}=L_{r3}=$ 120μH,

and C_{r1} = 141nF. In order to make unbal-

$= C_{r2}$ $= C_{r3}$

anced experimental condition, the value of the second mod-ule's resonant inductance, L_{r2} , changes 10% less than others ($L_{r2}=$ 108μH).

A. Experimental Waveforms of the Proposed System

The experimental waveforms of the input voltage and current of the three-phase PFC rectifier are shown in Fig. 13. In order to verify PFC operation of the prototype PFC rectifier, the same phase input ac voltage is applied to the three bridgeless PFC rectifiers. Fig. 13(a) shows power factor control of the prototype rectifier at 25% of the rated load. Fig. 13(b) shows the input voltage and current waveforms under the rated load condition. In the figures, both the line voltage and current waveforms at light load and full load are almost in phase, which means the proposed PFC can control unity power factor without reference to load conditions.
Fig. 14(a) and (b) shows experimental waveforms of the pri-mary resonant current of the dc–dc converter under no load and full load conditions, respectively. They are measured under the balanced case of the resonant components. Each waveform has the same switching frequency with the phase difference of $2\pi/3$ for the three-phase interleaved operation. Moreover, the input
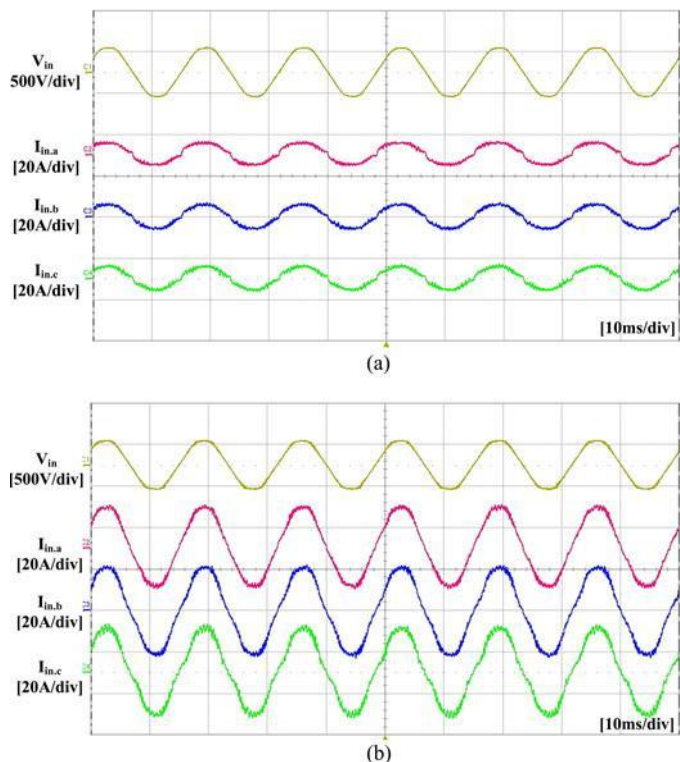
(a)

(b)

Fig. 13. Experimental waveforms of the input voltage and current of the three bridgeless PFC rectifiers: (a) At 25% load condition and (b) At full load condition.
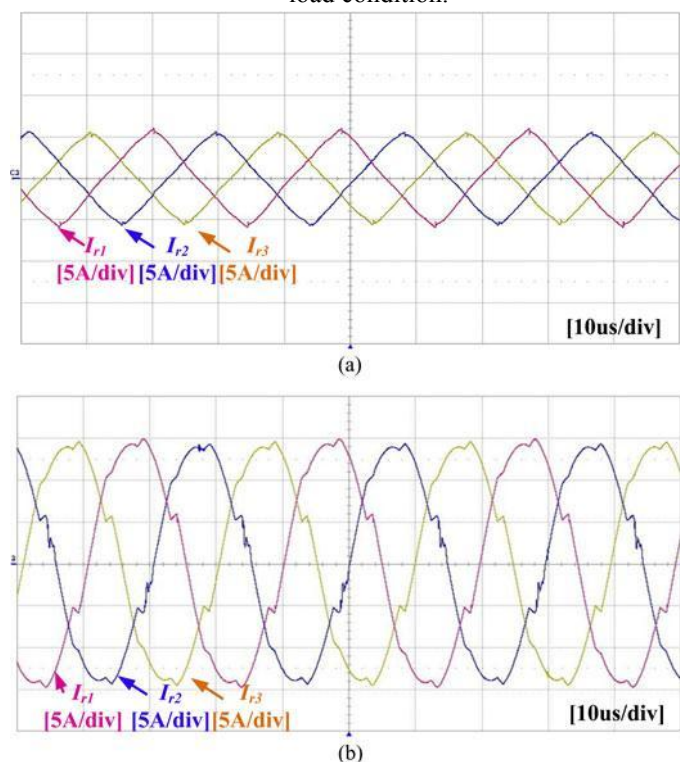

(a)

(b)

Fig. 14. Primary current of the proposed dc–dc converter:
(a) at no load condition and (b) at full load condition.

power for each converter is well balanced and they transfer the same amount of current from the primary side to the secondary side.

Fig. 15(a) and (b) shows experimental waveforms of the cur-rent and voltage of the primary and secondary stages of the dc–dc converter at light load (1 kW) and full load condition (10 kW) conditions, respectively. Due to the three-phase in-terleaved operation, the frequency of the output ripple of the rectifying current is as six times higher than the switching fre-quency. Using (5), the peak-to-peak ripple current of the rectifier can be calculated as 4.67 A at the full load. From the experimen-tal results, the actual value of the peak-to-peak ripple current was almost 4.7 A. In contrast, the conventional converter will have a ripple current around 50 A, as seen in Fig. 4(d). It shows that the ripple current at the output capacitor can be dramati-cally reduced using the interleaved operation. In addition, the primary resonant current, I_{r1}, is negative when VQ1 turns on. It verifies that the propose dc–dc converter can achieve ZVS operation under the entire load range.

B. Improvements of Current Balance and Efficiency

Fig. 16(a) shows the rectifying current passing through the output filter capacitor under the unbalanced condition of the 10% reduction of the primary resonant inductance at the light load condition of 1 kW. The peak-to-peak ripple current of the rectifier was measured to be 2.3 A. Fig. 16(b) shows waveforms of the peak to peak output ripple current using the proposed
balancing method. The value of the peak to peak ripple current was almost 1.3 A. From the experimental results, the peak-to-peak ripple current was decreased about 43.5%. Fig. 17(a) shows the rectifying current under the unbalanced condition at the heavy load condition of 8 kW. The peak- to-peak ripple current of the rectifier was measured to be 6.5 A. Fig. 17(b) shows waveforms of the peak-to-peak output ripple current us-ing the proposed balancing method. The value of the peak-to-peak ripple current was almost 3.7 A. In the experiment, the peak-to-peak ripple current was decreased around 43.1%. Using the proposed current balancing algorithm, the output voltages of the bridgeless PFCs can be controlled. The difference of the resonant gain among LLC resonant converters was compensated and the unbalanced output rectifier current was regulated. As a result, the ripple current at the output capacitor can be reduced using the proposed current balancing algorithm.

VI. CONCLUSION

To improve the power conversion efficiency for the dc distribution system, the high efficiency isolated ac–dc high-frequency-link-power-conversion system is proposed. The pro-posed system is composed of the bridgeless PFC rectifier with SiC diodes and the three-phase interleaved full-bridge LLC res-onant converter with the Y-connected rectifier. In addition, the output current balancing method for the three-phase interleaved LLC resonant converter is proposed. From the experimentalresults using the 10-kW (300 V/33.3 A) prototype converter, the validity and effectiveness of the proposed converter and the current balancing algorithm have been verified. Under the 10% unbalanced condition of the proposed dc–dc converter, the proposed balancing method can reduce the peak-to-peak ripple current about 41% at 1 kW and 29% under 8-kW load conditions. The proposed dc–dc converter shows high-power conversion efficiency of 97.88% at the rated load of 10 kW. Consequently, the power conversion efficiency of the proposed ac–dc high-frequency-link power conversion system is 95.53% at the rated load and it is improved 0.13% using the proposed current balancing method.

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